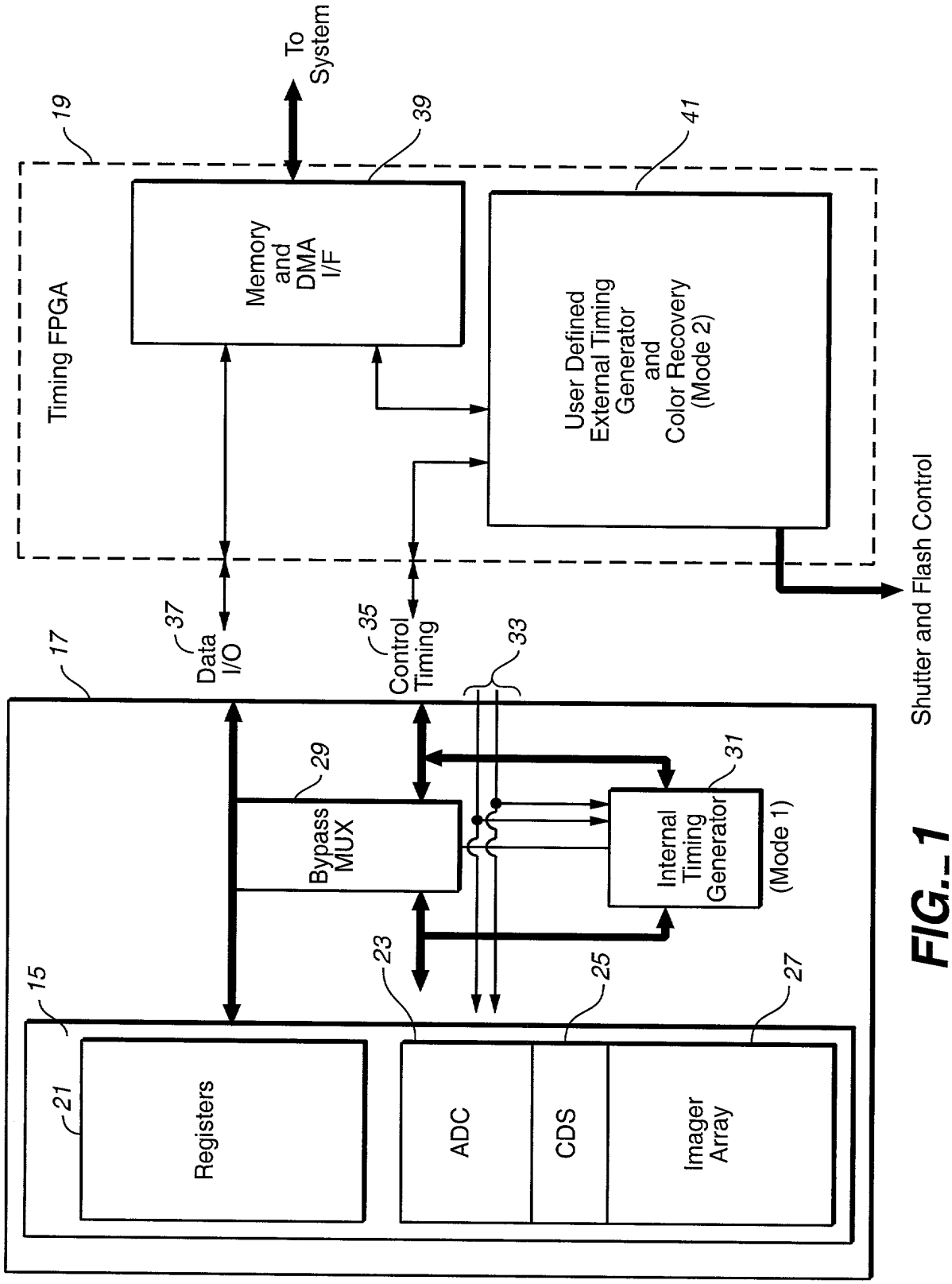
To System
19
39
41
Timing FPGA
Memory and DMA I/F
User Defined External Timing Generator and Color Recovery (Mode 2)
Shutter and Flash Control
37
Data I/O
35
Control Timing
33
17
29
Bypass MUX
31
Internal Timing Generator
(Mode 1)
23
25
27
15
21
Registers
ADC
CDS
Imager Array

FIG._1

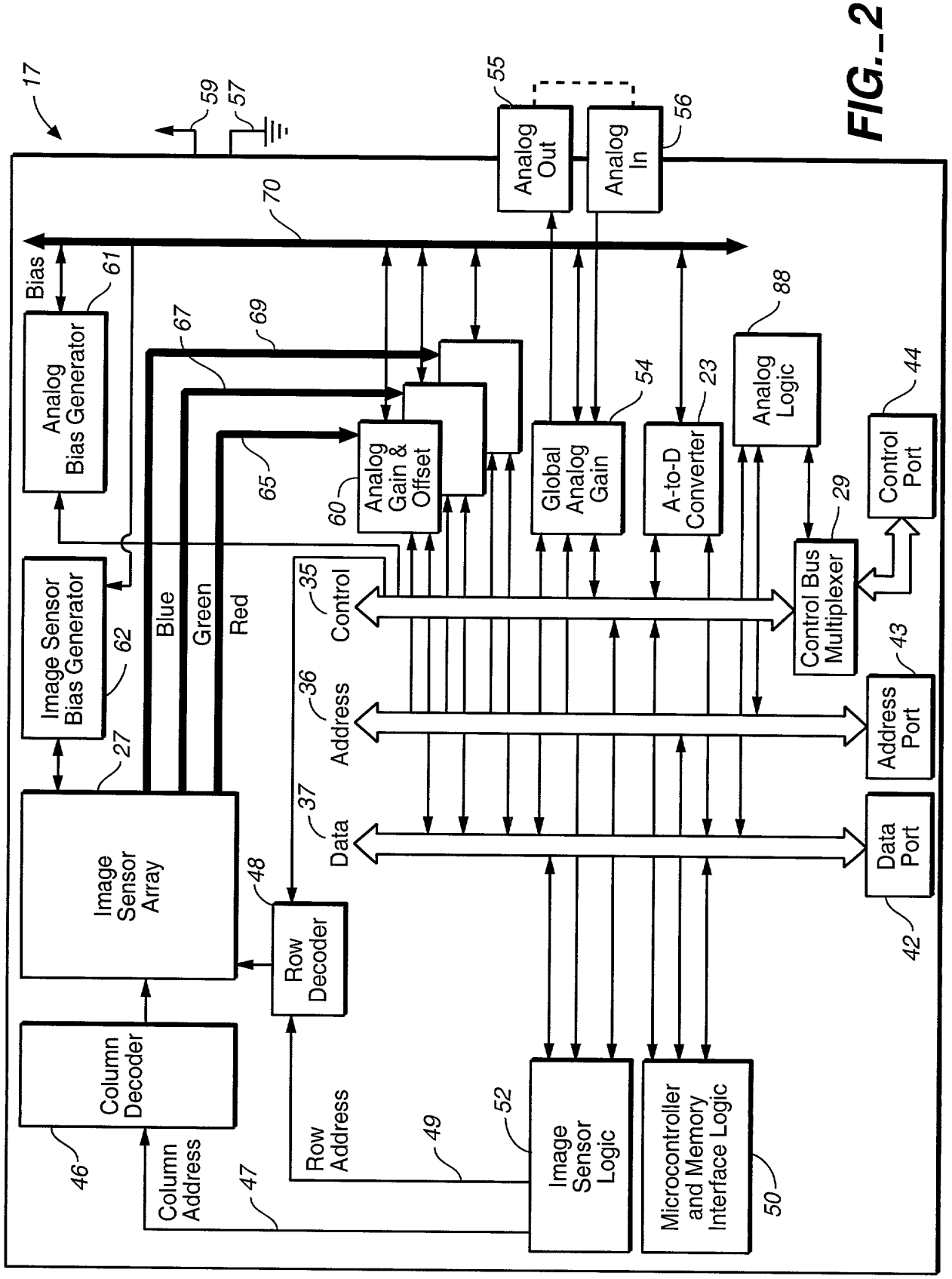
17
59
57
55
Analog Out
Analog In
56
70
Bias
61
Analog Bias Generator
67
69
Blue
Green
Red
65
60
Analog Gain & Offset
54
Global Analog Gain
23
A-to-D Converter
88
Analog Logic
44
Control Port
29
Control Bus Multiplexer
35
Control
Image Sensor Bias Generator
62
27
36
Address
43
Address Port
37
Data
Data Port
42
Image Sensor Array
48
Row Decoder
Column Decoder
46
Column Address
47
Row Address
49
52
Image Sensor Logic
Microcontroller and Memory Interface Logic
50

FIG._2

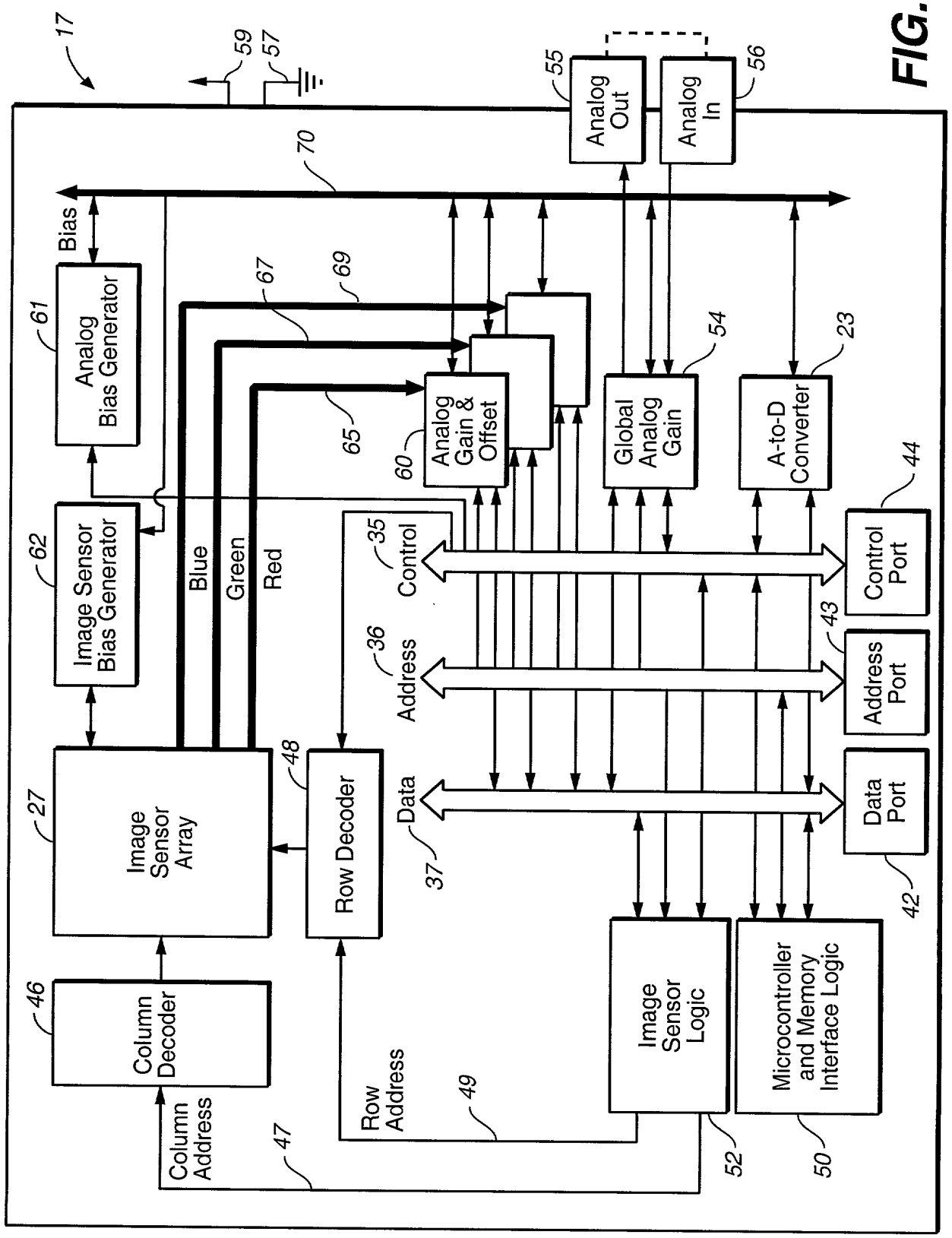
17
59
57
55
Analog Out
Analog In
56
70
Bias
61
Analog Bias Generator
67
69
65
60
Analog Gain & Offset
54
Global Analog Gain
23
A-to-D Converter
62
Image Sensor Bias Generator
Blue
Green
Red
35
Control
44
Control Port
36
Address
43
Address Port
27
Image Sensor Array
48
Row Decoder
Data
37
Data Port
42
46
Column Decoder
Image Sensor Logic
Microcontroller and Memory Interface Logic
Row Address
49
Column Address
47
52
50

FIG._3

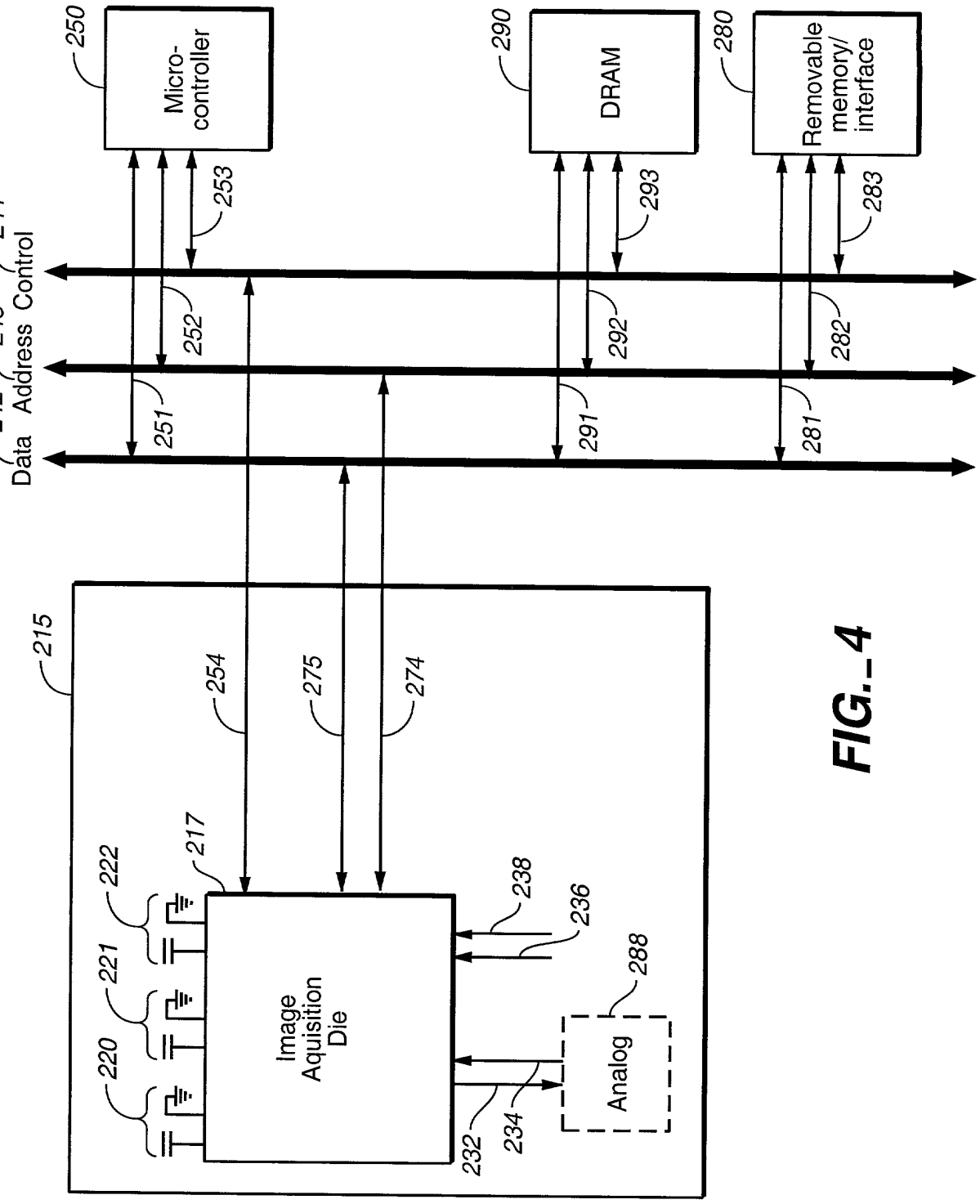
250
Micro-controller
290
DRAM
280
Removable memory/ interface
253
293
283
244
Control
243
Address
242
Data
252
292
282
251
291
281
215
254
275
274
217
222
221
220
238
236
288
Image Aquisition Die
Analog
232
234

FIG._4

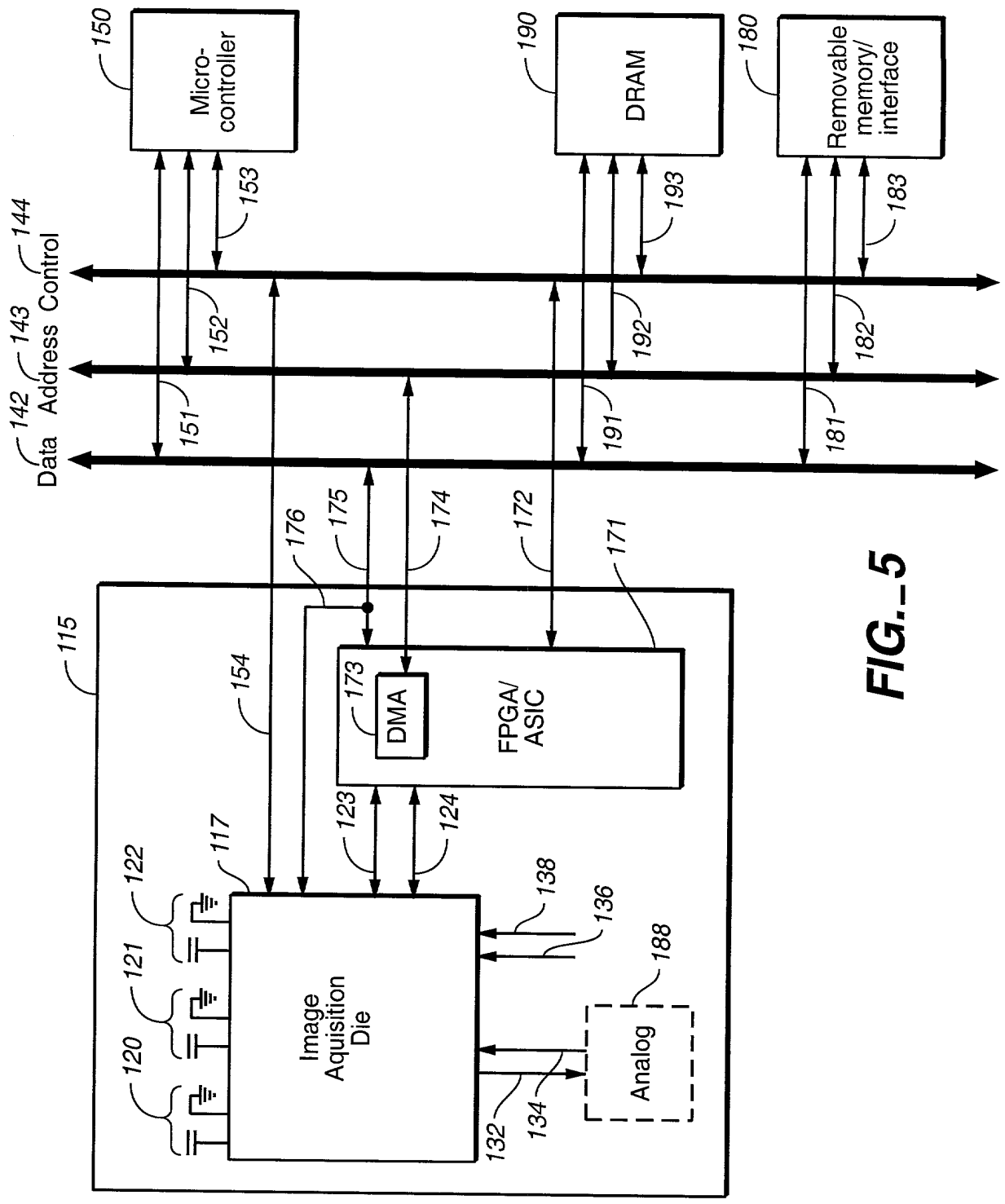
150
Micro-controller
190
DRAM
180
Removable memory/ interface
153
193
183
144
Control
143
Address
152
192
182
142
Data
151
191
181
176
175
174
172
171
115
154
173
DMA
FPGA/ ASIC
123
124
117
122
121
120
138
136
188
Image Aquisition Die
Analog
132
134

FIG._5

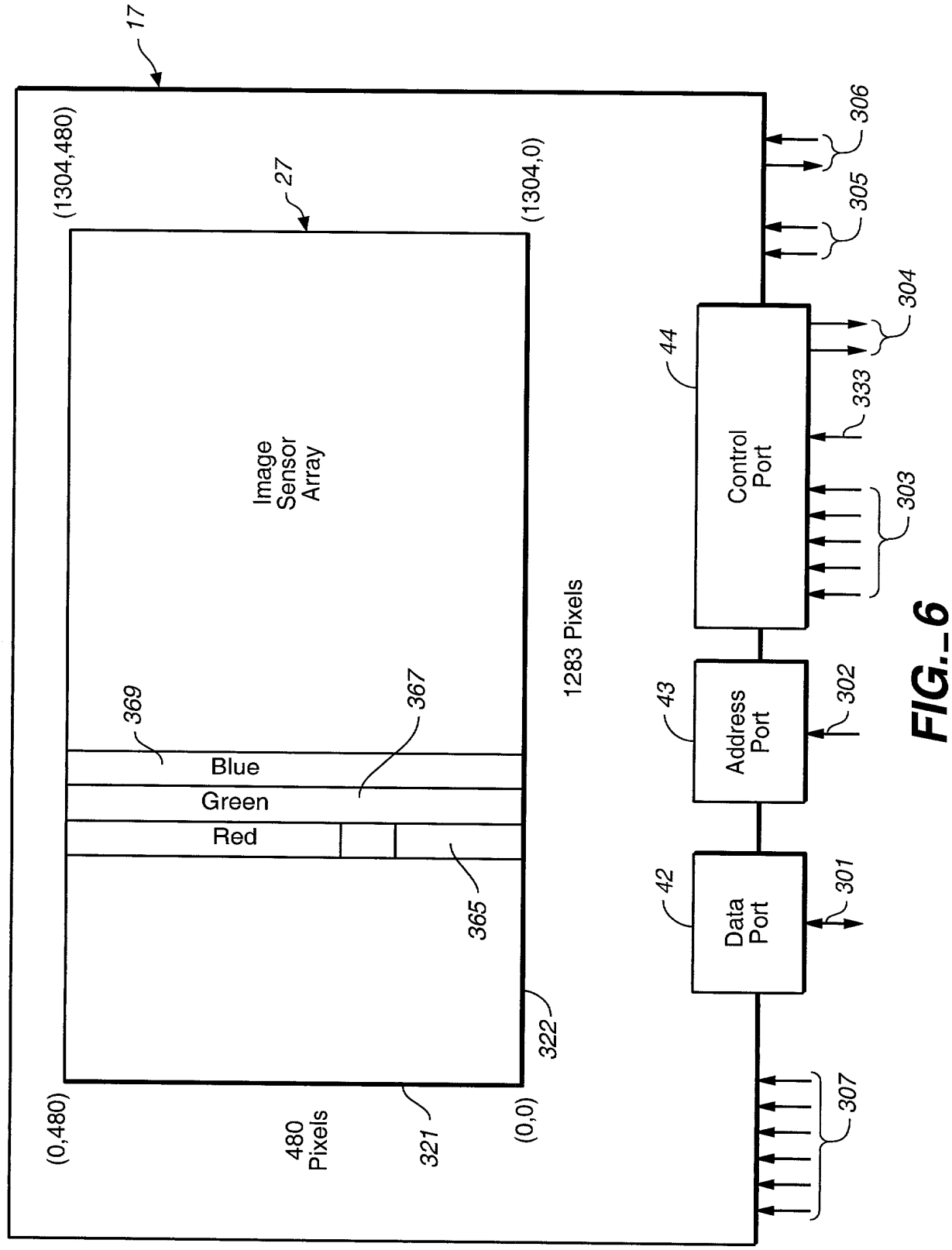
17
(1304,480)
27
(1304,0)
Image Sensor Array
1283 Pixels
369
367
Blue
Green
Red
365
322
(0,480)
480 Pixels
321
(0,0)
306
305
304
44
Control Port
333
303
43
Address Port
302
42
Data Port
301
307

FIG._6

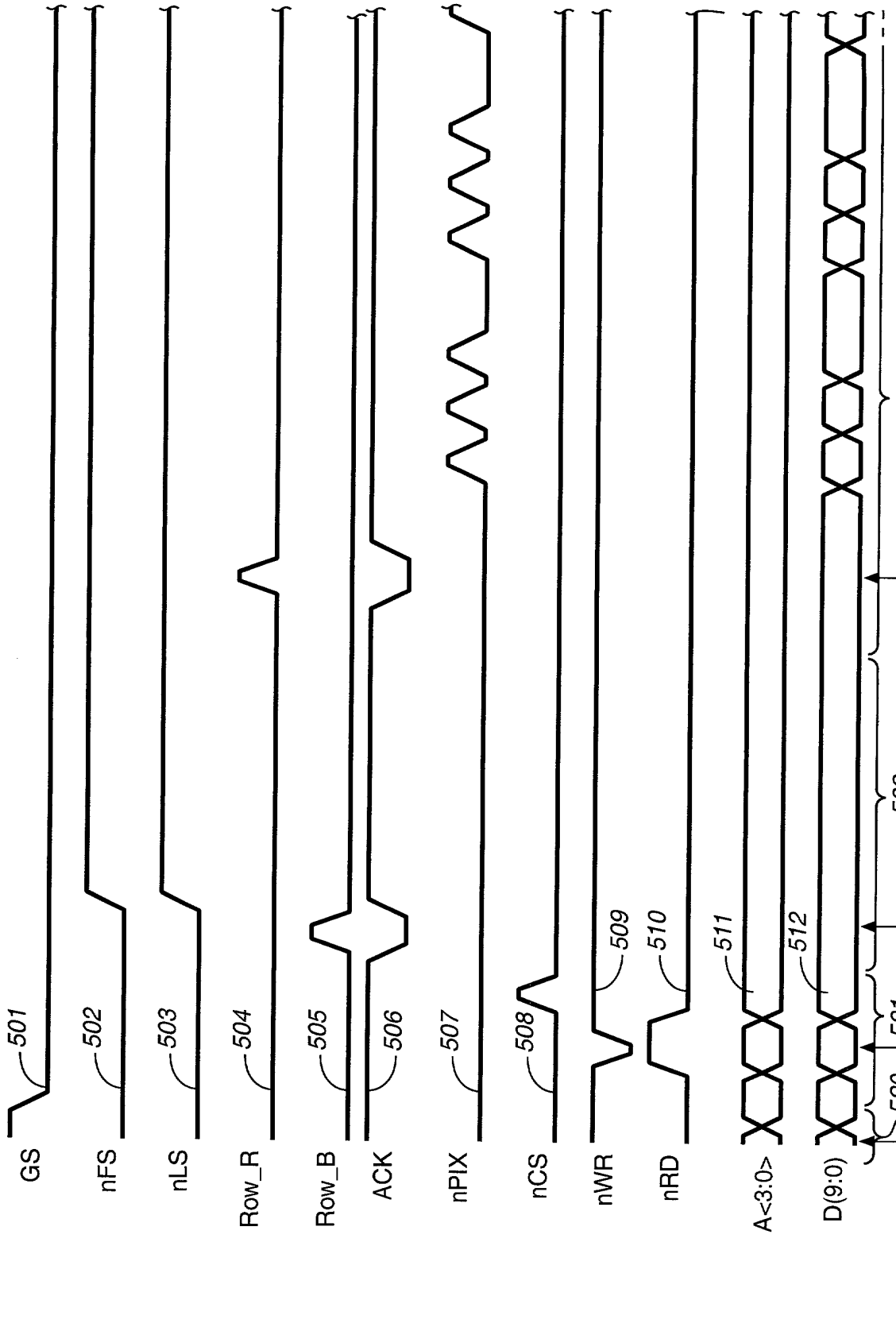
GS
nFS
nLS
Row_R
Row_B
ACK
nPIX
nCS
nWR
nRD
A<3:0>
D(9:0)
501
502
503
504
505
506
507
508
509
510
511
512
520
521
522
523
GS
Register Write
Start of Row Blanking
Start of Row Read (Line Read)

FIG._7

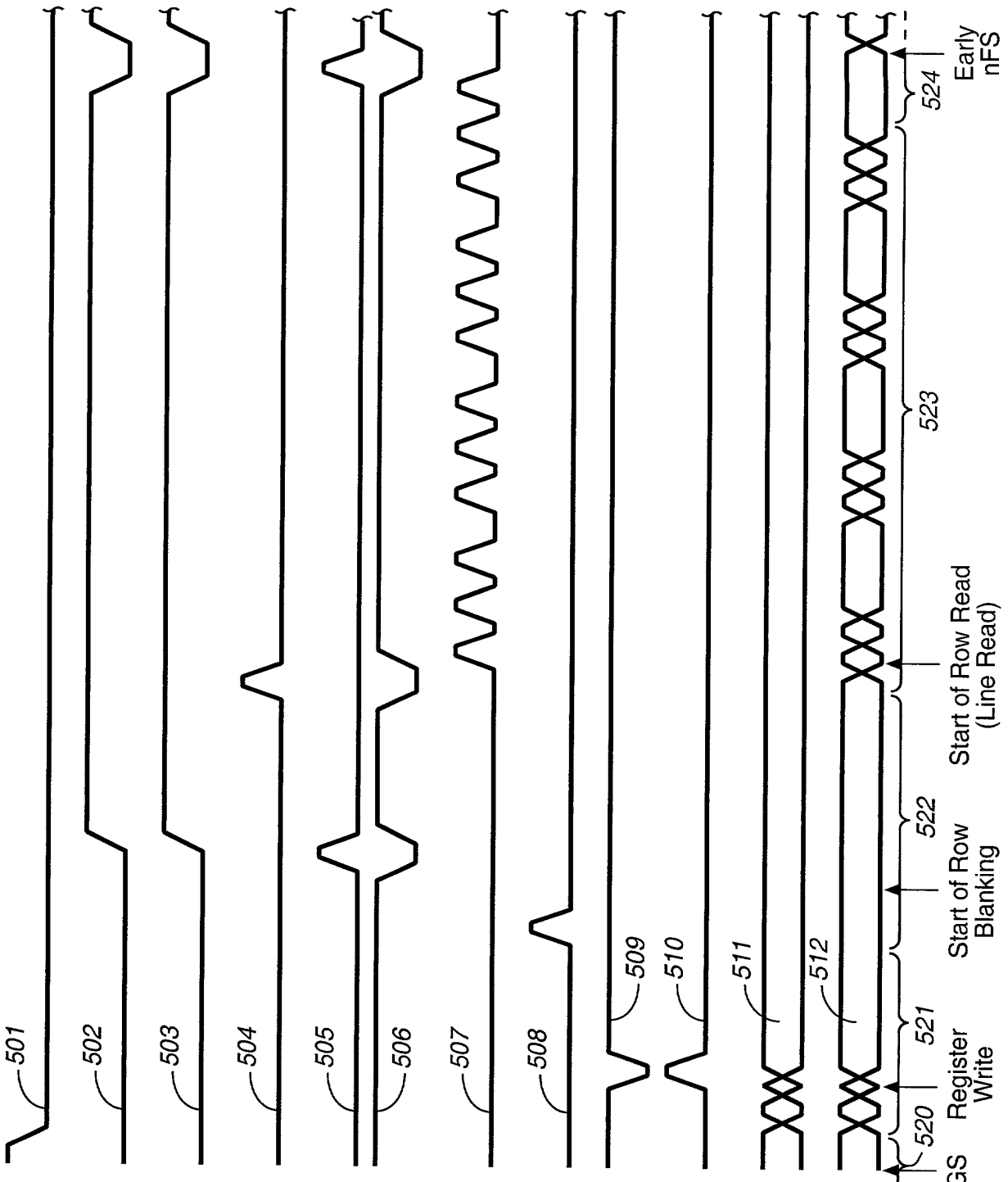
GS
nFS
nLS
Row_R
Row_B
ACK
nPIX
nCS
nWR
nRD
A<3:0>
D(9:0)
501
502
503
504
505
506
507
508
509
510
511
512
520
521
522
523
524
GS
Register Write
Start of Row Blanking
Start of Row Read (Line Read)
Early nFS

FIG._8A

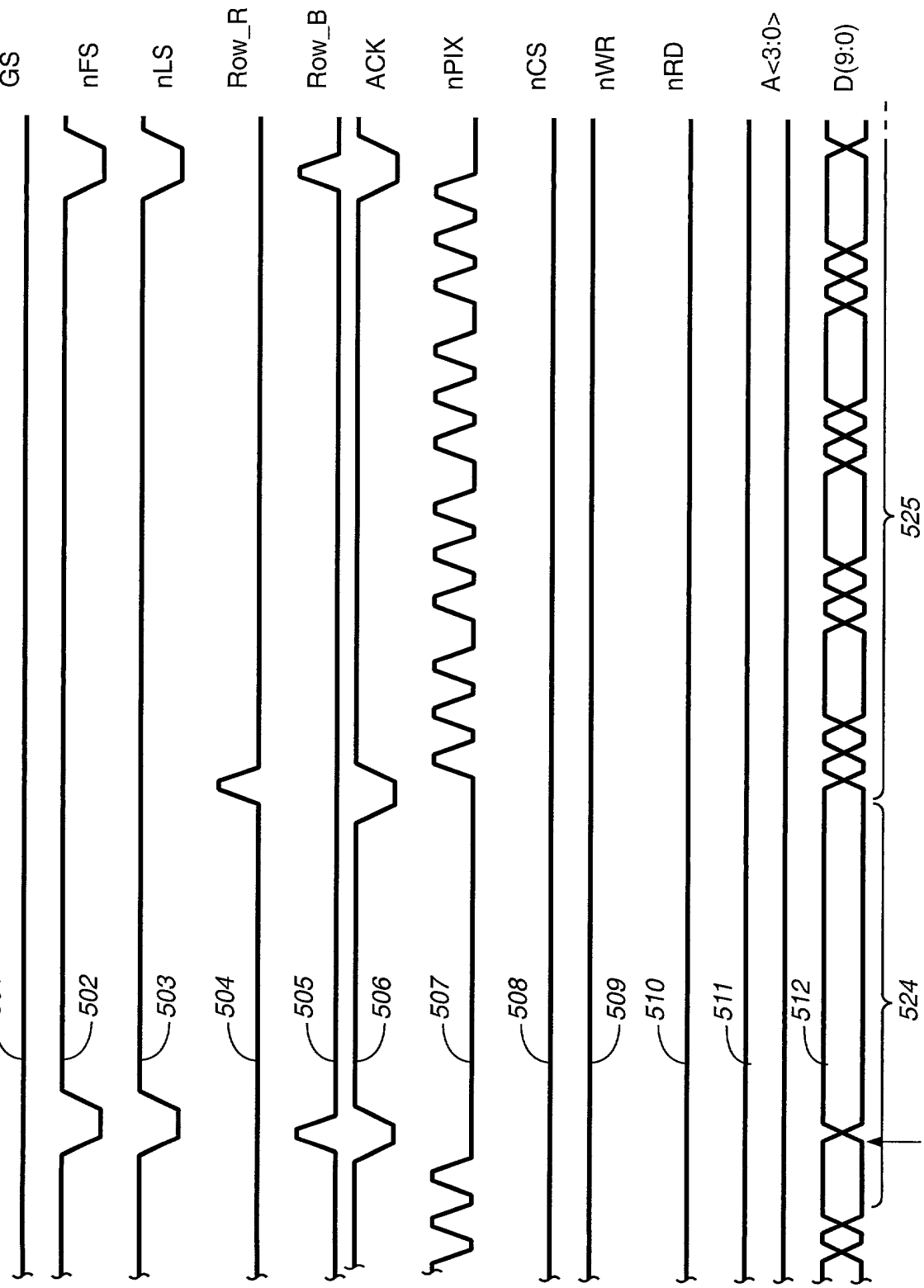
GS
nFS
nLS
Row_R
Row_B
ACK
nPIX
nCS
nWR
nRD
A<3:0>
D(9:0)
501
502
503
504
505
506
507
508
509
510
511
512
524
525
Early nFS

FIG._8B

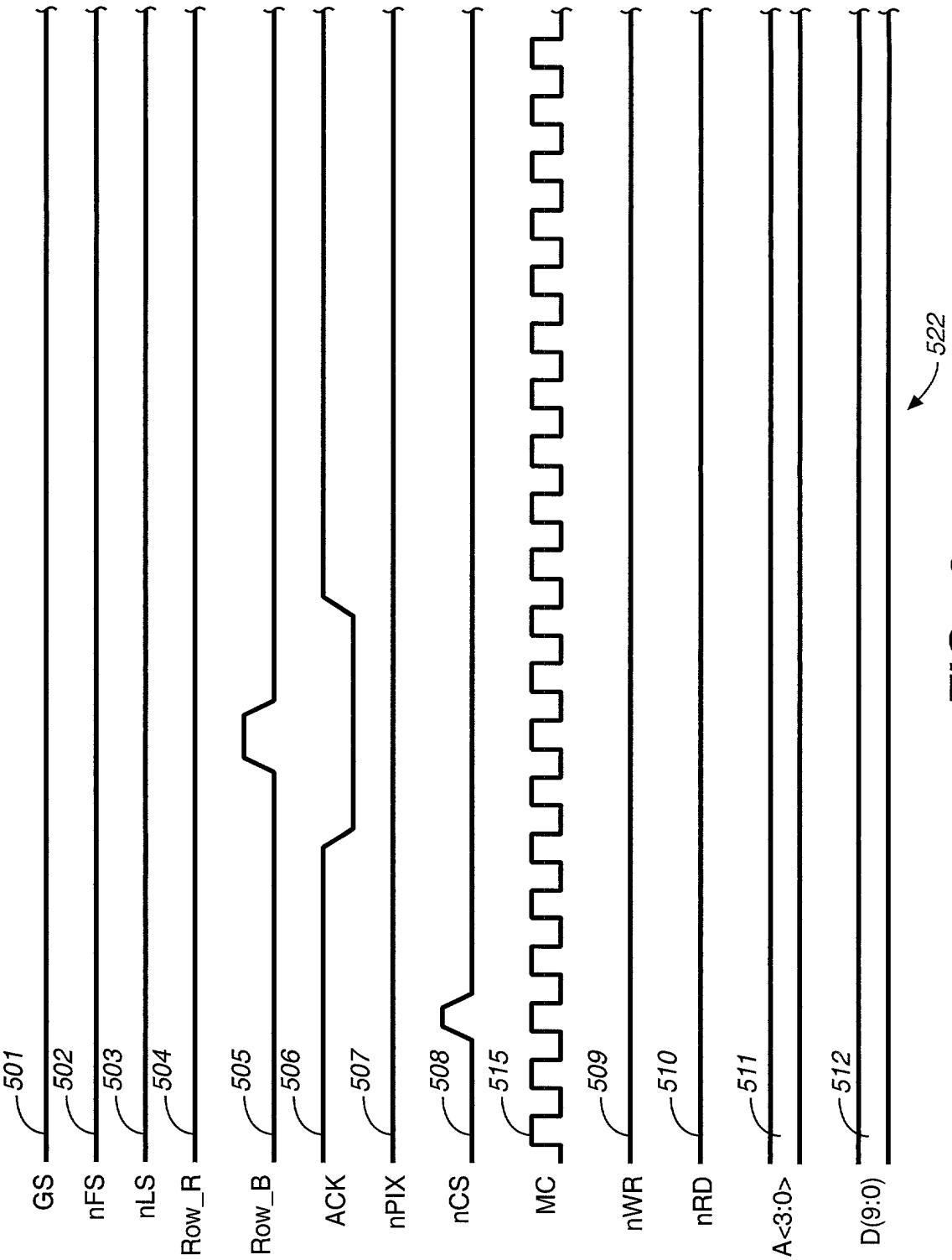
GS
nFS
nLS
Row_R
Row_B
ACK
nPIX
nCS
MC
nWR
nRD
A<3:0>
D(9:0)
501
502
503
504
505
506
507
508
515
509
510
511
512
522

FIG._9

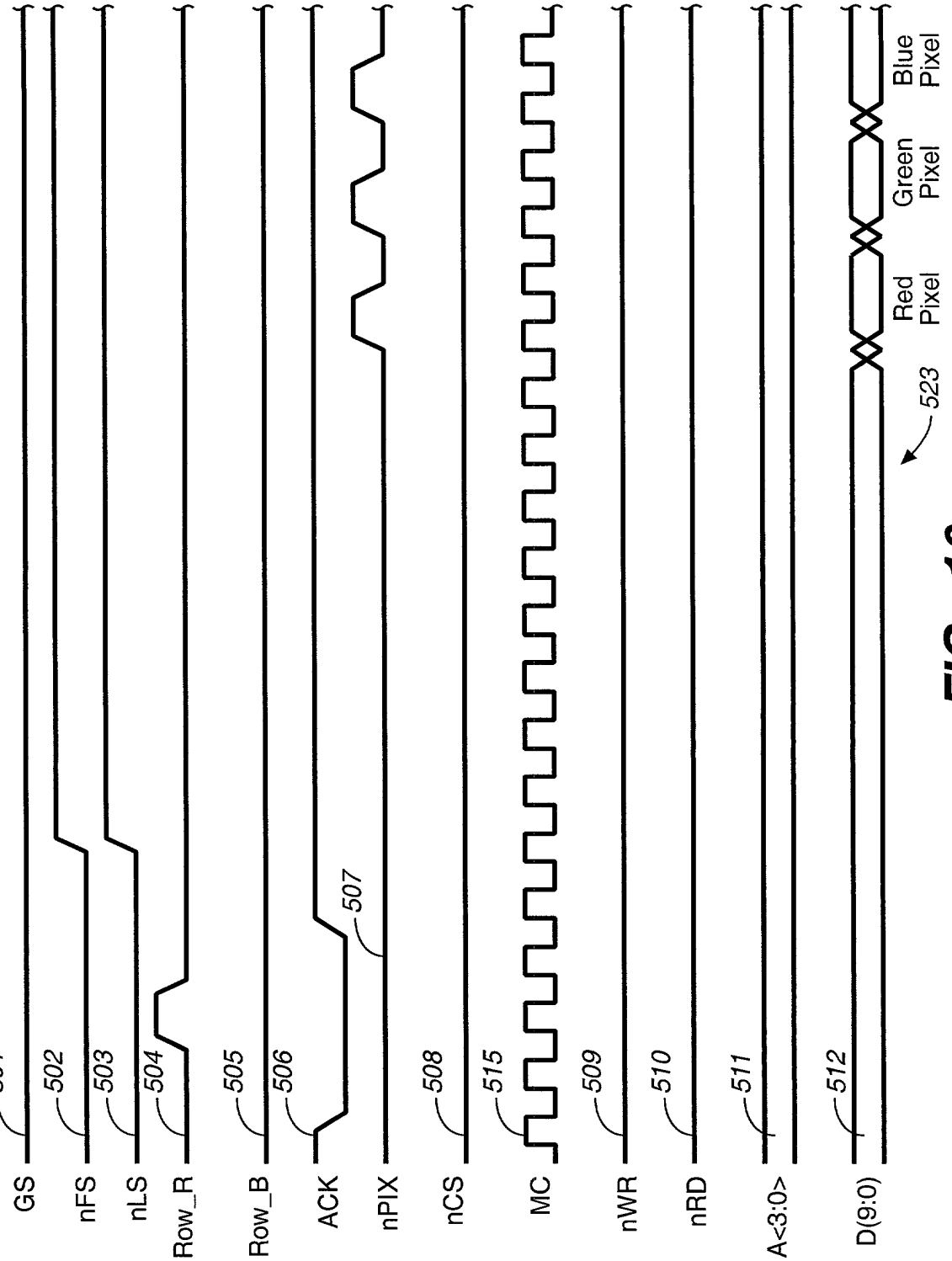
GS
nFS
nLS
Row_R
Row_B
ACK
nPIX
nCS
MC
nWR
nRD
A<3:0>
D(9:0)
501
502
503
504
505
506
507
508
515
509
510
511
512
523
Red Pixel
Green Pixel
Blue Pixel

FIG._10

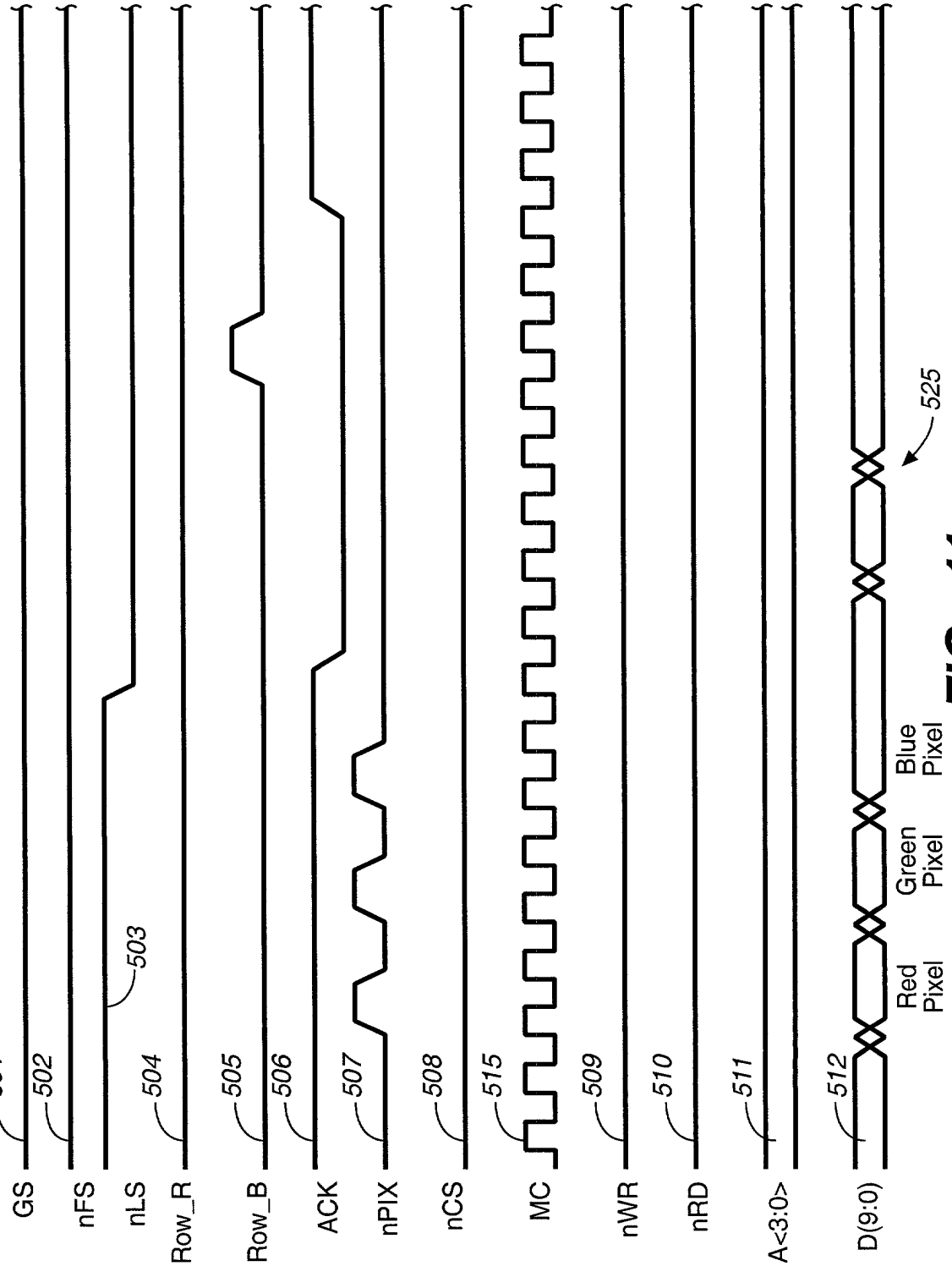
GS
nFS
nLS
Row_R
Row_B
ACK
nPIX
nCS
MC
nWR
nRD
A<3:0>
D(9:0)
501
502
503
504
505
506
507
508
515
509
510
511
512
525
Red Pixel
Green Pixel
Blue Pixel

FIG._11

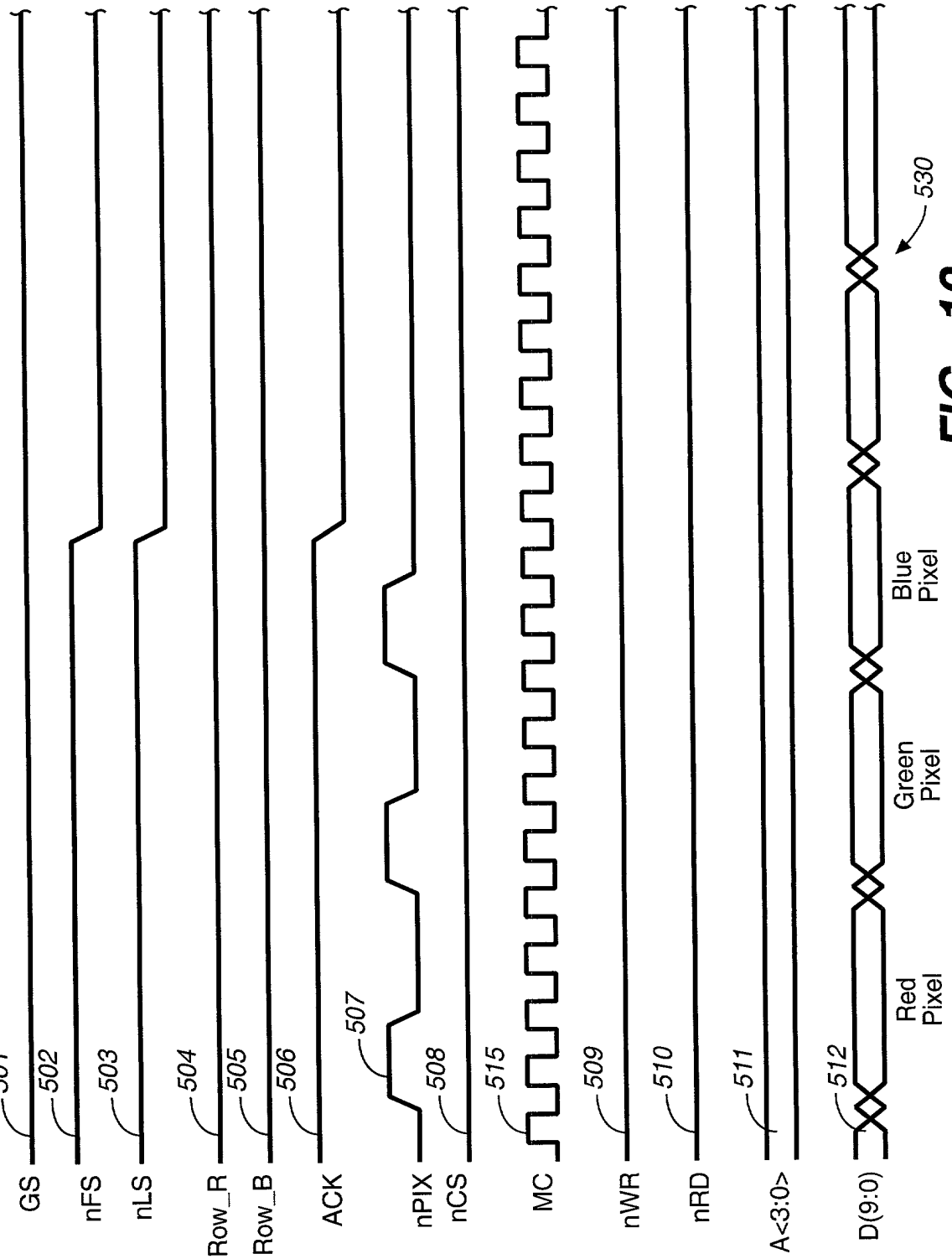
GS
nFS
nLS
Row_R
Row_B
ACK
nPIX
nCS
MC
nWR
nRD
A<3:0>
D(9:0)
501
502
503
504
505
506
507
508
515
509
510
511
512
530
Red Pixel
Green Pixel
Blue Pixel

FIG._12

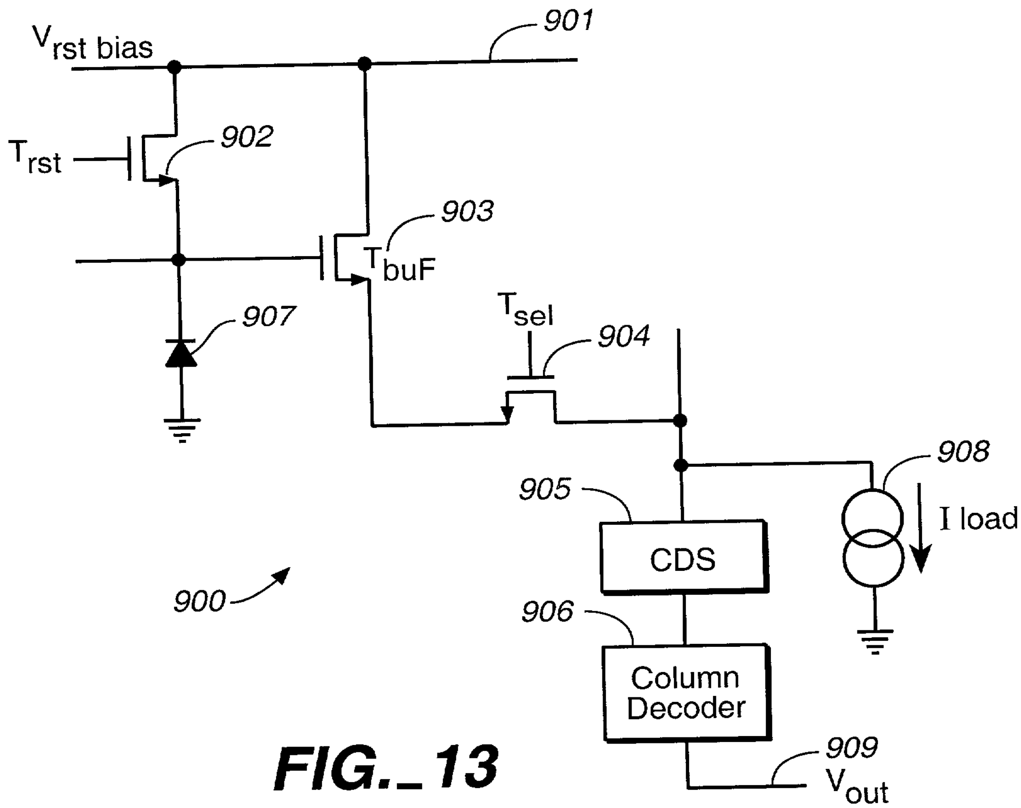

FIG._13

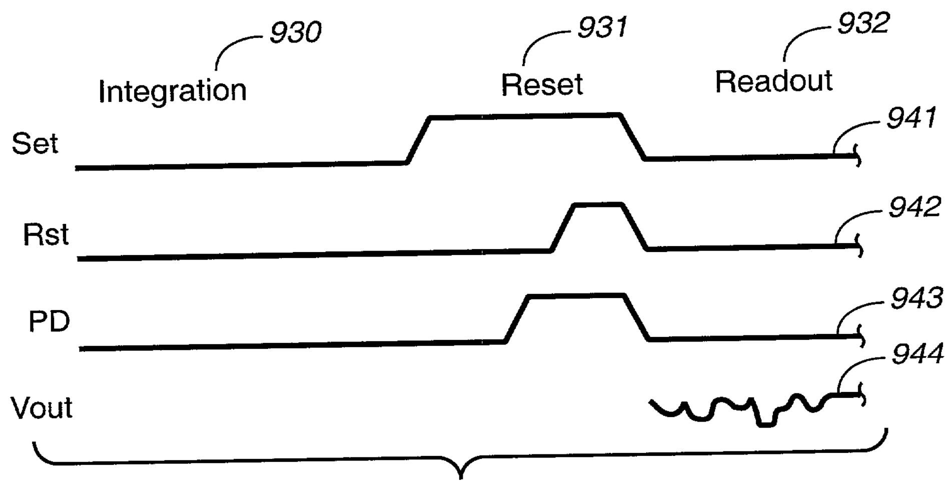

FIG._14